Lesson 17: Building a Hierarchical Design

Lesson Objectives

After you complete this lesson you will be able to:

- Explore the structure of a hierarchical design
- Editing the Training Root Schematic
- Making Power Pins Visible

Hierarchical Design

When you embed a schematic folder inside another schematic folder, you have created a hierarchical design. The process requires a block symbol, which represents a schematic or functional model. When the block symbol is used once in a schematic, the result is called a *simple* hierarchy (shown in the accompanying diagram). When the block symbol is used two or more times, the design is called a *complex* hierarchy.
More Information

The root schematic represents the top of the hierarchy, and is displayed in the Project Manager window with a slash on the folder icon.

A hierarchical design has several advantages. Its block diagram structure clearly shows how the functional units interact, and each block can be reused in the same or future designs. When you edit a block, all instances of the replicated block are changed throughout the hierarchical design.

Complex Hierarchical Designs

In a complex hierarchical design, OrCAD Capture automatically maintains multiple copies of the schematic in its database, one for each time it is referenced.
Connectivity in Hierarchical Designs

In flat designs, all the schematic pages are at the same level. You establish inter-page connectivity by terminating nets with off-page connectors.

By contrast, hierarchical designs have what might be called nested functionality embedded in schematic pages. Hierarchical block symbols on one schematic page reference more detailed design descriptions (other schematics or VHDL models).

More Information

The hierarchical pins on the block symbol and the hierarchical ports in the schematic (or VHDL file) are used to establish connectivity between the schematic folders in a hierarchical design.
Hierarchical Pins and Port Types

There are eight types of hierarchical ports, each with its own corresponding hierarchical pin type (as shown in the accompanying illustration).

To establish connectivity, a hierarchical pin must have a matching hierarchical port with the same Name and Type.

Adding a Port Symbol
In OrCAD Capture, there are eight port symbols to choose from. The symbol names relay information to the user about the direction in which the port is pointing (graphically), and the location of the pin (connection point). For example, *PORTLEFT-R* is a port symbol that points to the left, with a pin on the right. You may need to rotate port symbols before you place them.

**More Information**

You need to name the port to establish connectivity between the wire on the port, and the hierarchical pin on the block symbol. You can enter the name while placing the port, or change the name after you have placed it.

When adding a port, you must specify the port type. The port type provides a logical description of the net it represents (for example, input, output, or bidirectional).

Each of the eight symbols has a default type setting. You can select the port type while placing it, or change it after it has been added.

<table>
<thead>
<tr>
<th>Port symbols</th>
<th>Default type</th>
</tr>
</thead>
<tbody>
<tr>
<td>PORTBOTH-L</td>
<td>Bidirectional</td>
</tr>
<tr>
<td>PORTBOTH-R</td>
<td></td>
</tr>
<tr>
<td>PORTLEFT-L</td>
<td>Output</td>
</tr>
<tr>
<td>PORTLEFT-R</td>
<td></td>
</tr>
<tr>
<td>PORTNO-L</td>
<td>Passive</td>
</tr>
<tr>
<td>PORTNO-R</td>
<td></td>
</tr>
<tr>
<td>PORTRIGHT-L</td>
<td>Input</td>
</tr>
<tr>
<td>PORTRIGHT-R</td>
<td></td>
</tr>
</tbody>
</table>
Hierarchical Design Methods

Some degree of automated design supports either a bottom-up or top-down design flow. If you create additional hierarchical ports in the schematic or additional pins in a hierarchical block symbol, use the *Synchronize Up* or *Synchronize Down* command to re-link the data.
Lab 17-1: Explore a Hierarchical Design

Lab Objectives

After completing this lab you will be able to view schematics within the Training design and begin to understand how hierarchical designs flow.

(Due to the length of this lesson on Hierarchical design, it will be broken down into 3 sections or parts.)

Opening the Training Project

1. Select File - Open - Project.
2. Navigate to the D:\EMA_Training\Capture\training directory and open the training.opj file.
3. In the Project Manager window, double click on \training.dsn to expand the contents of the design file.
   Observe that the design contains three schematic folders (Training Root Schematic, Data Schematic, and HSRAM).
4. Observe the forward slash on the folder icon for the Training Root Schematic.
   The forward slash indicates the schematic is the ‘root’ or top level of the hierarchy.
5. Click the plus (+) signs next to each of the schematic folders to display their contents.
   Each of these folders contains a single schematic page, except the Training Root Schematic, which has two.

Viewing the Training Root Schematic

1. In the Training Root Schematic folder, double click on Page2.
2. Enlarge the schematic window, and zoom to all.
3. In the schematic window, locate the hierarchical blocks named High Speed Memory and Data Schematic.
   You will now push through these block symbols to display their lower level schematics.
Viewing the High-Speed Memory Schematic

1. In the schematic window, click on the High Speed Memory block symbol.
2. Right-click and select Descend Hierarchy from the pop-up menu.
   A second schematic window opens to display the HSRAM schematic. This is the circuitry that the hierarchical block represents.
3. Close the High Speed Memory schematic window.
   The Training Root Schematic window should still be open.

Descending through a block symbol can also be done by double-clicking in the selected block symbol.

Viewing the Data Schematic

1. In the schematic window, click on the Data Schematic block symbol.
2. Right-click and select Descend Hierarchy.
   A second schematic window opens to display the Data Schematic.
3. Close the Data Schematic window.
4. Close the Training Root Schematic window also.

In this lesson, you will work with the Training Root Schematic and Data Schematic only.
Lab 17-2: Editing the Training Root Schematic

Lab Objectives

After completing this lab you will be able to:

- Add a ground pin to a connector
- Add a bus and wiring
- Place a hierarchical port symbol
- Add an off-page connector
- Place a capacitor

Opening the Training Root Schematic

1. In the Training Root Schematic folder, double click on PAGE1.
2. Enlarge the schematic window, and zoom to fit.

Adding GND to Connector J1

1. Locate the 64-pin connector (J1) along the left side of the page.
   Observe that pins 1, 2, 3, and 33 are not connected.
2. There are several GND symbols already on this page. Copy one of them, and place it slightly to the right, center of the J1 connector, as shown in the following graphic near pin 33.
3. Click the Place wire icon.
4. Connect pins 1 and 33 to the GND symbol you placed in step 2.
   
   If necessary, use the <I>, <O>, and <C> keys to zoom in or out and pan while adding the wire.
5. Notice that when you connect a pin, the unconnected box at the end of the pin disappears.
6. Draw wires from pins 2 and 3 as shown in the graphic below.

When a connection between two wires is made, a junction dot appears at the intersection.

7. Press <Esc> twice.
8. Save the design.

Adding the BA[0-7] Wires

The Training Root Schematic, PAGE1 contains six FCT16245 parts as shown in the graphic below. Three of these parts are missing connections. In this lab you will be adding a BA[0-7] bus to the three parts identified by black arrows.
The graphic that follows shows the BA[0-7] bus you will be adding as you complete this lab. Your schematic should match this schematic after you complete this section of this lab.
1. Starting with one of the **FCT16245** parts, add a wire segment to pin **12**. Then press **<F4>** to replicate the segment, as shown in the following graphic.
2. Assign the net alias, **BA0**, to the bottom wire connected to pin 2.
3. Move the cursor up to the other wires and click each wire.

The alias automatically increments from the starting number, **BA0** to **BA7**, as shown in the next graphic.
4. Press `<Esc>` twice.

5. Place a bus entry on the **BA7** wire. If necessary, use the `<R>` key to rotate it before placing (as shown in the next graphic).
6. Press the `<Esc>` key once, then press the `<F4>` key seven times to replicate the bus entry on wires `BA6` through `BA0`.

7. Press `<Esc>` to exit the command.
8. Drag a rectangle around the new connections, right-click, and select **Copy** from the pop-up menu (or **CTRL + C**).
9. Press `<Esc>` to deselect, then right-click and select `Paste` (or `CTRL + V`).
10. Place copies of these connections on the other two `FCT16245` parts.

If you have `Options - Preferences - Select - Intersecting` enabled, be sure the rectangle does not touch any pins on the part, or they will be selected also. (The `Fully Enclosed` selection option may be useful in these kinds of situations.)

11. Save the design.

**Adding the BA[0-7] Bus**

1. Click the `Place bus` icon.
2. Press and hold the `<Shift>` key and draw the bus wire, as shown in the example at the beginning of this lab.
   
   Holding the `<Shift>` key lets you draw diagonal segments.

Adding the net alias `BA[0-7]` to the bus wire is not necessary if the Bus is attached to an `Off-Page Connector` or an `Hierarchical Port` symbol. But, it is necessary if it is NOT attached.
**Placing a Hierarchical Port Symbol**

1. Click the **Place port** icon. The Place Hierarchical Port window appears.
2. In the Libraries list, click on **CAPSYM**.
3. From the Symbol list, select **PORTRIGHT-L**.
4. In the **Name** field, enter **BA[0-7]** and click **OK**. DO NOT place it yet.

5. Right-click and select **Edit Properties** from the pop-up menu. The **Edit Hierarchical Port** window appears.
6. Set the **Type** field to *Output* and click **OK**.
7. Attach the port symbol to the end of the bus wire.
8. Press `<Esc>` to exit the command, and `<Esc>` again to deselect the port.
9. Save the design.

You can also place the generic port symbol and edit the name and port type at a later time. Both ways are correct.

**Adding Off-Page Connectors**

1. Locate the **20L10** part in the upper right corner of the page.
2. Use this example and the following steps to add the **Off-page Connectors** shown below.

3. Choose the **Place off-page connector** icon.
4. In the Place Off-Page Connector window, select **OFFPAGELEFT-R** from the **CAPSYM** library.
5. In the **Name** field, enter: **HS/**
6. Click **OK**.
   
   The connector is pointing left.
7. Press `<R>` twice to rotate it to point right.
Beware of “special characters”. Some Netlisters for other board layout tools will not accept them. For the OrCAD and Allegro PCB Editor, the only ones to avoid are “!” and “’”. However, avoid spaces in net names, design names and directory names.

8. Place the symbol near the pin 19 of the 20L10 part. Remember to leave at least one grid space to add a wire to the symbol.

If you place the symbol directly on the pin, a connection is automatically created between the pin and the off-page connector. However, if you intend to place properties on the net you must have a wire segment. Properties are placed on Parts and Wires. If you move the off-page connector, a wire will appear connecting it to the pin.

9. Repeat this operation to place five more Off-page Connectors.

After placing each connector, press <Ctrl+E> and use the Edit Off-Page Connector window to specify the name of the next connector to be placed. Use the names listed within the graphic of step 2.

10. Where necessary, place a wire segment between the Off-page Connectors and the pins of the part.
11. Save the design.

**Placing Capacitors**

1. Zoom into the area shown below.
2. Click the **Place part** icon on the schematic editor toolbar.

3. When the **Place Part** window opens, where it lists the Libraries, click on **DISCRETE**, select **CAP** from the Part List, and hit the **Enter** key. DO NOT place the part yet.

4. Right-click and select **Edit Properties**.
   a. In the **Value** field, enter: 
      
      0.1\mu F
   b. In the **PCB Footprint** field, enter: 
      
      SM_1206

5. Click **OK**.

6. Place four capacitors, as shown in the following graphic.
7. Press `<Esc>` twice.
8. Add wires, as shown in the example above.
9. Copy existing VCC and GND symbols and complete the circuit.
10. Save the design.

**Making Power Pins Visible**

*Reasons for Over-riding Pin Connections*

When a part is built in the library, its power pins can be defined to be invisible (default) or visible when used in a design.

A power pin that is visible in the design must be explicitly wired to the appropriate voltage net. However, an invisible power pin is connected implicitly to a power net having the same name as the pin. (No explicit wire connection is needed in the design.)

In some designs, it is necessary to override the implicit voltages defined within the invisible power pins on a device. For example, you may want the power pin to connect to “+5V” or “-12V”. To override the voltage of an implicit (invisible) power pin, you must make the pin visible.
Reasons for overriding implicit power pin connections with explicit connections in the design include:

- The design might not have a default power bus, so you must connect the pins to explicit power nets.
- You might want to connect power pins to a power bus or net other than the default power bus for such purposes as noise isolation, power distribution, and so on.
- The default pin name may differ from the system’s power and ground net names.
Lab 17-3: Making Power Pins Visible

Lab Objectives

After completing this lab you will be able to edit the visibility attribute of power pins.

1. In the upper right corner of the page, double click on the 20L10 part.
   The Property Editor appears.

2. Locate the Power Pins Visible property.

3. Click the Power Pins Visible checkbox, in the “white” column, as shown in the graphic that follows.

4. Close the Property Editor window.

5. Press <Esc>, and zoom in to view the part.
   The power pins on the 20L10 part are now visible (top and bottom).

6. Copy a VCC symbol and connect it to pin 24 (at the top of the 20L10 part).

7. Copy a GND symbol and connect it to pin 12.
Remember, if you are using the “short” pin graphics, draw the wire from the symbol then double-click on the pin end to make it attach.

The Secondary or “yellow” column shown in the Property Editor will be explained later in the lesson.
Saving the Design

1. Select **File - Save** to save the schematic page.
2. Select **File - Close** to close the schematic window.