Lesson 19: Processing a Hierarchical Design

Lesson Objectives

After you complete this lesson you will be able to:

- Annotate a hierarchical design
- Perform a Design Rule Check on a hierarchical design
- Correct your design (if needed)

Processing a Hierarchical Design

Instances versus Occurrences

An *instance* is a part that appears once in a design. An instance of a part is found in a flat or simple hierarchical design.
An occurrence applies to complex hierarchical designs only. When a block symbol occurs more than once in a hierarchical design, the schematic it represents also occurs multiple times. (Each instance in the schematic occurs multiple times, one “occurrence” in each block.)

More Information

In the accompanying illustration, the DAAMP Circuit occurs twice, referenced by two hierarchical blocks in the Data Schematic. When you edit a part in the DAAMP Circuit, the Property Editor shows the instance properties in white and the properties on each occurrence in yellow.

When processing a hierarchical design, each occurrence of a part must be processed. For example, the Annotate program must assign a part reference to each occurrence in a duplicated block. Occurrence mode is required to properly annotate your design, run Design Rules Check, cross reference your parts, and create a Bill of Materials.

In a complex hierarchical design, the Property Editor will show different Part Reference property values for each occurrence.
Checking Hierarchical Ports

Use *Design Rules Check* to flag any hierarchical port naming or direction errors. You can request a list of all port names used in the design. Whenever a net name override occurs, the losing net is listed as an alternate. Always check the list of alternate net names in the DRC report.

More Information

Within each schematic folder, hierarchical ports take precedence over all other types of connections in the schematic. From highest to lowest, the precedence levels are listed in the table that follows.
<table>
<thead>
<tr>
<th>Design Object...</th>
<th>Takes precedence over...</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hierarchical port</td>
<td>All other types of connections.</td>
</tr>
<tr>
<td>Off-page connector</td>
<td>A net alias or a voltage symbol.</td>
</tr>
<tr>
<td>PWR/GND symbol</td>
<td>A net alias. When multiple voltage symbols are wired together, the lowest net (alphanumerically) takes precedence.</td>
</tr>
<tr>
<td>Net alias</td>
<td>An unlabeled wire. When multiple net aliases are wired together, the lowest net (alphanumeric ally) takes precedence. Will inherit its name from an off-page connector.</td>
</tr>
<tr>
<td>Unlabeled wire</td>
<td>The lowest level of connectivity is an unlabeled wire. The system generates a default net name.</td>
</tr>
</tbody>
</table>

When you create a netlist for PCB design, the hierarchy is “flattened”. This means that the highest level of connectivity, at the highest level in the hierarchy, takes precedence in the netlist. A net alias on a wire at the top (or root) of the hierarchy will override the port symbol name in the lower level schematic. (The net name from the root schematic is passed down into the schematic below.)
Lab 19-1: Annotating the Design

Lab Objectives

After completing this lab you will be able to:

- Annotate all schematic folders
- View part references as an instance (flat design) and occurrence (hierarchical design)

Annotating Schematic Folders

1. In the Project Manager window, click on \training.dsn and select Tools - Annotate.
2. In the Scope section, make sure the Update Entire Design option is selected.
3. In the Action section, be sure Incremental Reference Update is selected.
   This option only assigns part references to parts that do not already have part references assigned. Since the J1, J2, and J3 connectors are already annotated, and we do not want to change their assignments.
4. In the Mode section, the Update Occurrences option should be selected by default. If not, select it now. (See the following selections.)
5. Click **OK** to annotate the design, and **OK** to continue.

The design is annotated and saved to disk.

When annotating a hierarchical design, OrCAD Capture annotates first in the root schematic folder, then in other schematic folders connected hierarchically to the root folder.
Getting Started with OrCAD Capture

OrCAD Capture Version 16.6

Viewing Part References as an Instance and Occurrence

1. Open **PAGE1** of the Data Schematic.
   Observe that all the parts in this page now have part references assigned.
   a. Select the **DAAMP1** block symbol, right-click, and select **Descend Hierarchy**
      (double-click or press <SHIFT+D>).
      The underlying schematic is displayed. Observe some of the part references assigned
      to the parts in this schematic.
   b. Right-click and select **Ascend Hierarchy**.
   c. Now descend into the **DAAMP2** block.
      You now have schematics for both **DAAMP** blocks open.

2. Use the **Window** pull-down menu to toggle between the two occurrences of the **DAAMP** Circuit schematics. They are the same schematic, but with different part
   reference assignments.
   Because there are two **DAAMP** block symbols in the design, the parts in each of those
   **DAAMP Circuit** schematics occur more than once in the hierarchical design. This is
   known as complex hierarchy, and is the reason OrCAD Capture differentiates
   between “instances” and “occurrences”.

3. Close all three schematic windows.
4. In the Project Manager window, double click **PAGE1** of the schematic page in the
   **DAAMP Circuit** folder.
5. Observe that you are prompted for a specific occurrence of the schematic page
   (**DAAMP1** or **DAAMP2**) as shown in the graphic that follows.

6. Select the **Data/DAAMP1** entry and click **OK**.
   The schematic associated with the **DAAMP1** block symbol is displayed.
7. Close the schematic window.
8. In the Project Manager window, click on .\training.dsn and save the design.
Lab 19-2: Running Design Rules Check

Lab Objectives

After completing this lab you will be able to check a hierarchical design for design rule violations.

Selecting Settings within the Design Rules Check Dialog Box

1. Highlight `.\training.dsn` in the Project Manager window.
3. In the Design Rules Check window, enter the settings shown in the following pictures.
4. Make sure you have
   D:\EMA_Training\Capture\training\training.drc listed below
   View Output. If not, type it in or use the Browse button to add that directory.

5. Select the Electrical Rules tab next. Use the following settings.
6. Select the Physical Rules tab next. Enable the following settings.
7. Click **OK**.

The DRC report is displayed.

**Reviewing the DRC Report**

This report contains five different sections, one for each of the schematic folders in the design. These five sections are:

- Training Root Schematic
- HSRAM
- Data_Schematic
- DAAMP1/DAAMP Circuit
- DAAMP2/DAAMP Circuit

Take note of the sections within the report that contain warnings. OrCAD Capture generates **DRC** markers on the schematic pages where errors and warnings are occurring.
1. Close the **DRC** report window.

In the Project Manager window, observe that the `.\training.drc` file was added to the **Outputs** folder.
Lab 19-3: Correcting Your Design (If required)

Lab Objectives

After you complete this lab you will be able to:

- Identify DRC error markers
- View and identify errors in the schematic
- Fix the errors within the schematic

Browsing for DRC Error Markers

1. Click on Training Root Schematic in the Project Manager window.
2. Select Edit - Browse - DRC Markers.
   The DRC errors for the Training Root Schematic appear in a Browse DRC Markers window.
3. Place your cursor between the column headings, and drag the mouse to increase the column width.
   The data in each column is now clearly visible.

Observe that the data is sorted by the DRC error column (all the common error messages are grouped together).
4. Click on the **Page** column heading to sort the error messages by page number.
5. Click on the **DRC Detail** column heading to sort the error messages by design object.

Observe that the net names involved in the error messages are almost the same (except for the forward slash). In an earlier lab you added off-page connectors to page one of the Training Root Schematic. Per the lab instructions, you named these off-page connectors **BRD/**, **BWR/**, **FPGA/**, and **HS/**.

### Viewing the Errors in the Schematic

1. Double click an error message containing the **BRD/** net name. (You must double click in the **DRC Error** column.)
   
   Page one of the *Training Root Schematic* opens, and the error you selected is highlighted.

2. Zoom into the area containing the **DRC** error markers as shown below.

   ![Diagram of DRC error markers]

   Another way to get information about an error message is to open the page and double click on an error marker.

### Fixing the Training Root Schematic

1. Click on the **BRD/** text to the right of the off-page connector, right-click, and select **Edit Properties** (you can also double click).

2. Remove the forward slash character from the off-page connector name and click **OK**.

3. Do the same thing for the **HS/**, **FPGA/**, **BWR/** connector names.

4. Save the design.

5. Close the schematic page, and click **No** at the prompt to close the open window.
Saving the Design

1. In the Project Manager window, click on .\training.dsn and select File - Save.
2. Click on the design file again, and select Tools - Design Rules Check and click OK.
3. The report should be free of the error messages you just corrected.