Lesson 12: Preparing for Post Processing

Learning Objectives

In this lesson you will:

- Rename reference designators on the board design
- Backannotate changes made in the OrCAD and Allegro PCB Editor to DE CIS

In this section you will learn about preparing your design for post processing. This will include automatic and manual renaming of reference designators, and backannotating your design changes to your schematic.
Design Layout Process

This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. The items about to be discussed are sometimes included in the manufacturing output area.
Renaming Reference Designators

You can rename your reference designators and backannotate to your schematic at any time in the design process. After renaming, you would want to backannotate your schematics. Renaming and backannotation are presented here mainly to present a consistent flow and also as another point during which you may want to perform these tasks.

It is not uncommon to rename (resequence) the reference designators on a board at the end of the layout phase. The process results in a physical layout that is easier to test, debug, rework, assemble, and maintain in the field. A particular component is easier to locate when reference designators on the board are ordered in a consistent and predictable fashion (such as left to right, top to bottom).

Caution

Before attempting to rename components in the OrCAD and Allegro PCB Editor, it is advisable to contact the engineer you are working with to get a copy of his most recent schematic. He might have changed the circuitry. If that is the case, and you change the reference designator names, the two will be out of sync. Therefore, before changing reference designators or swapping functions or pins, be sure to forward annotate the schematic to be certain you are working with current information.
The automatic renaming process in OrCAD and Allegro PCB Editor lets you rename every component on a design in a single operation. You can also elect to rename individual components by attaching the AUTO_RENAME property to them, or rename components on one side of the board only.

Renaming is controlled by placement grid line locations only (user-defined or default selection) or by sequential renaming within grid blocks. With grid-based renaming, you can designate the direction (horizontal or vertical) and order (left-right, right-left, upwards-downwards) of the renaming process. Additionally, you can define grid descriptions by alpha characters and/or integers.

To access automatic renaming tools in OrCAD and Allegro PCB Editor, select \textit{Logic - Auto Rename RefDes}.

\textbf{Rename Reference Designators Main Form}

Use the following steps to automatically rename your components:

\begin{enumerate}
\item Choose \textit{Logic - Auto Rename RefDes} from the top menu.
\item Choose the type of placement grid you want to use.
\begin{itemize}
\item \textbf{User Defined Grid} - You define a grid on the class BOARD GEOMETRY and subclasses PLACE_GRID_TOP and PLACE_GRID_BOTTOM. The system will use these grids, looking at each grid square based upon the direction specified in the Rename RefDes Setup Form (see next page).
\end{itemize}
\end{enumerate}
– **Use Default Grid** - This option basically results in no two parts ever being considered in the same block for renaming purposes.

3. Select which components to rename.

– **Rename All Components** - Renames all components on the side of the board specified in the Rename RefDes Setup Form (see next topic).

– **Attach Property, Components** - You must attach the property AUTO_RENAME to all components that are to be renamed in this pass.

4. Click **More...** to check or change sequencing parameters (see next topic).

5. Click **OK** in the Rename RefDes menu to begin execution.

**Rename Reference Designators Setup Form**

Select the **More** button to bring up the Rename Ref Des Setup form. You use this second form to set the parameters used when running the rename reference designator command.

The **Layer Options** section of this form specifies whether to rename the top side, bottom side, or both sides of the design. You also specify the origin point of the part for renaming purposes.

Use the **Directions for Top Layer** and **Directions for Bottom Layer** sections of this form to specify the rename order for the appropriate layer.
Use the **Reference Designator Format** section to specify how the new reference designator names should be created. The Ref Des prefix field specifies what the starting character or characters of the new name should be. An asterisk in this field specifies that the reference designator format as defined in the library footprint symbol should be used as the starting character or characters of the new name. If you want to keep the current prefix as was defined from the schematic, use an asterisk in this field, and check the box titled Preserve Current Prefixes. Use the fields Top Layer Identifier and Bottom Layer Identifier to specify a character that will be appended to the new reference designator name on the appropriate layer. Use the field Skip Characters to identify the characters that should not be included when creating a new reference designator name.

The Renaming Method field can be set to either Sequential or Grid Based. If you choose the sequential method, the **Sequential Renaming** section becomes available. Use the field Ref Des Digits to specify the minimum number of digits that should be used when creating a new reference designator name. For example, if 2 is specified, the numbers following the reference designator prefix would be 01, 02, 03 and so forth.

If you choose the Grid Based method, the **Grid Based Renaming** section becomes available. You use the **First Direction Designation** and **Second Direction Designation** fields to assign the prefixes to be used when creating the new reference designator name. Use the **Suffix** field if there is more than one component in the same grid cell. If you are going to use the grid based renaming method, you should use the User Defined Grid method as discussed above.

Once you have specified all the parameters in the Rename Ref Des SetUp form, select Close in this form. To execute the renaming sequence, select **OK** in the Rename Ref Des form.
Rename Reference Designators—Key Points

Things to Remember

- Before changing reference designators, verify the engineer and designer are using the schematic at the exact same stage of the design (no changes made to schematic)

- A component can be individually renamed by editing the attached reference designator (Edit - Text)

- An AUTO_RENAME property can be attached to specific groups of components to sequence them separately

- A HARD_LOCATION property can be used to prevent certain components from being renamed

- User-defined grid cells can be used to determine specific row and column boundaries

- There are many options available for determining number and letter sequencing (Refer to CDSDOC to find your best settings)

- Reference designators can only be changed ONCE between back annotations

- When you rename components, you MUST backannotate the changes to your schematic source

When you rename reference designators, there are a few things to remember. You can manually rename a part by changing the reference designator text. To manually change the reference designator, select the Edit - Text option from the top menu, select the reference designator to be renamed, and enter in the new reference designator on the OrCAD and Allegro PCB Editor command line. You can change the text on the assembly top, assembly bottom, silkscreen top, or silkscreen bottom subclasses under the class Ref Des. If there are certain parts that you do not want to be renamed by the auto rename tool, attach the property HARD_LOCATION to them. When you rename your components, you must backannotate your schematics with the reference designator changes to keep the schematic and the design in sync.

Caution

The rename reference designator process can only be run ONCE before back annotating the changes from the board design to the schematic capture environment. The back annotation process compares the reference designator in the original netlist files with the changed reference designator in the changed logic output files from the board editor. Running the process more than once breaks the link from the original reference designator to the reference designator you want to send back to the schematic.
Backannotation

Mapping changes from the physical layout back to the logical schematic world

- Property changes
- Ref-des changes
- Pin and gate swaps

If you rename the reference designators in your design, you will need to backannotate these changes to the schematic. In order for backannotation to work correctly, the schematic must not have been changed since the last logic import into the OrCAD and Allegro PCB Editor board or the last backannotation had been performed.
There are other changes that can be made that will require backannotation. The OrCAD and Allegro PCB Editor tool can perform gate and pin swapping, which can improve component placement and routing.

These processes—gate and pin swapping, and rename—represent changes to the OrCAD and Allegro PCB Editor database, and must be communicated back to the schematic.

Backannotation is capable of documenting reference designator and physical pin number changes only. To perform properly, the schematic and physical layout must match. If parts exist in the schematic that are not on the board (or vice versa), or schematic connectivity does not match the physical layout, these differences will be identified.
Integrating Logic Design with Physical Layout

**Design Entry CIS (DE CIS) Front End**

**DE CIS:** It is not required that the schematic reside in the same directory as the OrCAD and Allegro PCB Editor design. However, it is recommended that the two be kept together. The minimum values required on a DE CIS schematic library part are Value, Class, and Footprint (package symbol).

**Annotate:** The Annotate program converts the logic devices into physical packages, assigning a reference designator and physical pin numbers to each symbol in the schematic.

**OrCAD and Allegro PCB Editor Netlister:** The OrCAD and Allegro PCB Editor Netlister creates the transfer files used by OrCAD and Allegro PCB Editor. By default, these files are created in a directory named allegro.

**OrCAD and Allegro PCB Editor**

**Import Logic:** After this step has been completed, the design contains all of the connection information.

**OrCAD and Allegro PCB Editor:** Used for component placement and routing; allows for pin and gate swaps for optimum routing results; generates manufacturing output.
**Export Logic**: This program generates backannotation files that the DE CIS tools use to update the schematic.

### OrCAD and Allegro PCB Editor to DE CIS Backannotation

**OrCAD and Allegro PCB Editor**: 
*File - Export - Logic*

**DE CIS**: 
*Tools - Back Annotate*

The first step in backannotating from OrCAD and Allegro PCB Editor to DE CIS is to generate the feedback files. These are the same four `compView.dat`, `funcView.dat`, `pinView.dat` and `netView.dat` files used in the OrCAD and Allegro PCB Editor to DE HDL backannotation process. This can be done from within OrCAD and Allegro PCB Editor by using the *File - Export - Logic* command or by using the Generate Feedback Files option from the DE CIS *Backannotate* command.

After the four feedback files have been generated from the OrCAD and Allegro PCB Editor design, you must run the backannotation process from within DE CIS. This process will read the OrCAD and Allegro PCB Editor-generated feedback files, create an output swap file that contains all the required backannotation information required by DE CIS, and update the schematic.

Properties are passed back and forth between these two tools. You define which property names are allowed to pass. They are controlled by listing them in the `allegro.cfg` file located at `<cdsroot>/tools/capture`.
Labs

• Lab 12-1: Renaming Components
  – Use the renaming capability in the OrCAD and Allegro PCB Editor to setup resequencing and change reference designators

• Lab 12-2: OrCAD and Allegro PCB Editor to DE CIS Backannotation
  – Backannotate changes made in the OrCAD and Allegro PCB Editor physical layout to the DE CIS logical schematic

The following labs will allow you to:

  – Familiarize yourself with the process and steps required to automatically and manually rename your design.

  – Familiarize yourself with the process and steps required to backannotate your design to a DE CIS schematic.
Lab 12-1: Renaming Components

Objective: Assign new reference designators automatically and interactively, using the renaming qualifications.

Important

The labs refer to the course installation directory (where you uncompressed the database file) as the <course_inst_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course_inst_dir> directory with the name of your chosen directory.

Setting Colors and Visibility

1. If you don’t already have OrCAD and Allegro PCB Editor software running, start OrCAD and Allegro PCB Editor.

2. Open the file routed.brd.

3. Choose View - Zoom Fit from the top menu.

4. Choose Display - Color/Visibility from the top menu.

5. Select the Global Visibility Off button.

6. Select Yes to confirm change of visibility of all classes.

7. Select the Components/Ref Des folder.

8. Turn ON ASSEMBLY_TOP and ASSEMBLY_BOTTOM.

9. Select the Board Geometry folder.

10. Turn ON OUTLINE.

11. Select the PACKAGE GEOMETRY folder.

12. Turn ON ASSEMBLY_TOP and ASSEMBLY_BOTTOM.

13. Select the Stack-Up/Conductor folder.
   It is easier to see the reference designators with the wiring turned off.

14. Turn ON only the following:
    TOP-PINS, BOTTOM-PINS, TOP-VIAS and BOTTOM-VIAS.
15. Click OK to close the Color Dialog form.

**Renaming Components**


2. Check to see that **Use Default Grid** is selected.

3. Check to see that **Rename ALL Components** is selected.

4. Click on the **More...** button. The Rename RefDes Setup form appears.

5. Make adjustments to this menu to match the form:

Notice that the Top Layer Identifier and the Bottom Layer Identifier fields have been blanked out because we don’t want extra suffixes added to show what side the component is placed on. The Preserve Current Prefixes check box has been enabled to use the same format that is currently in the reference designators.
6. Click Close to return to the Rename RefDes Setup menu.

7. Click Rename to begin executing the automatic rename process.

8. Click Close to close the Rename RefDes form.

9. Zoom in or pan your view to inspect your results.

10. Choose File - Save As from the top menu.
    A browser form appears.

11. In the File Name field, enter:
    release

12. Click Save in the file browser.
    The file release.brd is saved to disk.
    You will overwrite this version of your design while preparing it for final output phases.

**Interactively Renaming Parts**

1. Zoom in to view a component of your choice.

2. Choose Edit - Text from the top menu.
    The OrCAD and Allegro PCB Editor message area prompts,
    Pick text to edit.

3. Click on the reference designator of the component you want to rename.
    The selected refdes is highlighted.

4. At the OrCAD and Allegro PCB Editor command line, enter:
    U99 (or any name you wish) and press Return.

**Note**
If the name you choose already exists in your design, you are notified in the
OrCAD and Allegro PCB Editor message area that the name is being swapped
with another component. This feature prevents you from accidentally creating
duplicate names.

5. To exit from the Edit - Text command, right-click and choose Done from the pop-up menu.
6. Choose *File - Save* from the top menu.
   
   A window appears and warns you that the `release.brd` file already exists. It asks if you want to overwrite the file.

7. Click *Yes* to confirm the overwrite.

   The file `release.brd` is written to disk.

**End of Lab**
Lab 12-2: OrCAD and Allegro PCB Editor to DE CIS Backannotation

Objective: Create backannotation files and incorporate them into the DE CIS schematic using a revised board database.

You have previously performed gate swapping and renamed your reference designators. These database changes must be sent back to the schematic.

Note
This lab is for designs that were created from a DE CIS schematic only!


2. Select Design entry CIS in the Logic Type folder tab if it is not currently selected.

3. In the Export to directory field, browse to the project2/allegro directory.

4. Click Export Cadence.
   The feedback files pinview.dat, compview.dat, netview.dat, and funcview.dat are created. These files can be used in the DE CIS backannotation process.

5. Select Close to close the Export Logic form.

End of Lab
Lab 12-3: Backannotation in DE CIS (Optional)

Objective: Backannotate OrCAD and Allegro PCB Editor changes into the DE CIS schematic.

If in a previous lab you had preferred to netlist directly from OrCAD Capture or OrCAD Capture CIS (DE CIS) into the OrCAD and Allegro PCB Editor rather than import the netlist in the OrCAD and Allegro PCB Editor you should do this lab to understand the process of back annotating the changes into the schematic.

1. Open the OrCAD Capture tool.
2. Open the release.opj project from within the project2 directory.
3. Select the release.dsn design file.
4. Choose Tools - Back Annotate....
   The Backannotation form appears.
5. Set the selections in the Backannotation form to match the picture below.

6. Click OK.
   The release.swp file is generated and read into the schematic and the changes are made in the schematic.

End of Lab